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PATENT APPLICATION
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Sir:

Transmitted herewith for filing is the patent application of:

Inventor: Sung Wook KIM et al
Title: METHOD FOR COMPRESSING OUTPUT DATA AND A PACKET COMMAND DRIVING TYPE MEMORY DEVICE

Enclosed are the following papers and documents required for filing date under 37 CFR 1.53(b):

15 Pages of specification
5 Pages of claim(s)
1 Pages of abstract
8 Sheets of drawing
___ Combined Declaration and Power of Attorney
___ An assignment of the invention to:
x A certified copy of a Korean (1999-24581) application
___ Verified Statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27
___ Assignment Recordation Cover Sheet with accompanying fee
x Other: Information Sheet

The filing fee has been calculated as shown below:

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FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	11 -20=	* 0
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Respectfully submitted,

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Date

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METHOD FOR COMPRESSING OUTPUT DATA AND A PACKET COMMAND DRIVING TYPE MEMORY DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a packet command driving type memory device, particularly, to a method for compressing output data that can reduce a test time and discriminate exactly a position which a fail is produced and a memory device having a pre-fetched data output structure.

Description of the Related Art

In a prior packet command driving type memory device, e.g., a memory device such as a RAMBUS DRAM, a data pass structure is drawn in Fig 1, Fig 2 is a detail drawing relating to A part(a dot line part) of Fig 1, is a drawing showing a pass through which data from a core cell region 10 to an output pad DQ are outputted.

When writing data, one bit data are transferred to an interface part 40 respectively, and data are packed by 8 bits during 4 clock cycless in a negative edge and a positive edge of each clock per each data pad(DQA0- DQA7, DQB0- DQB7). Even number data of 8 bits data packeted during 4 clock cycles, for example, are transferred to a data input, output part via an interface part 40 in an ascending edge of a clock signal tclk, odd number data, for example, are transferred to the data input, output part 30 via the interface part 40 in an ascending edge of a clock signal tclk.

The 8 bits data transferred via the interface part 40 are transformed to parallel data of 8 bits WD<0:7> through a data input shift part(not drawn in a drawing) of the data input, output part 30 and transferred to the core cell region 10 via

a column control part 20 and written in a packet form.

On one hand, when reading data, on the contrary, 8 bits data RD<0:7> read from the core cell region 10 in a packet form are transferred to the data input, output part 30 via a column control part 20, the data input, output part 30 transforms it to series data via shift registers 31-34, a multiplexer and drivers 41-44 of the interface part 40 transfer even number data eread<0, 2, 4, 6> in an ascending edge of a clock signal tclk, odd number data odd<1, 3, 5, 7> in a descending edge of a clock signal tclk, to a data pad. Accordingly, 8 bits series data are transferred in a packet form via respective data pads (DQA0- DQA7, DQB0- DQB7) during 4 clock cycles.

A prior memory device having a data pass structure as described above prefetched data by 8 bits from the core cell region 10, outputted data in accordance with an ascending edge and a falling edge of a clock signal via a shift register of the data input, output part 30.

However, a prior memory device having a data pass structure as described above checked out an output of every output data pad of a memory device and discriminated a fail of a device in a DA test mode, as a data output pass is separated every respective output data pin. Therefore, there was a problem that an efficiency falls when it is a test for mass producting numerous devices.

That is, the number of pins allocated for outputting data of a tester is N, when the number of data output pads of a device is 16, it was possible to test N/16 devices simultaneously at a time.

Also, a prior memory device compared the data read from the core cell region via a read data comparing part and discriminated whether a fail of a memory device is produced or not, thereby outputted the result(Error_out) via an output terminal SIO1 of one error. However, a prior memory device could discriminate whether a fail is produced by comparing the read data, but there was a improper problem in a wafer level test, that one can't

know where of a core cell region 10 a fail was produced, hence one has to seek a repair cell.

SUMMARY OF THE INVENTION

The present invention is invented to solve the problem of the prior art, it is an object of the present invention to provide a method for compressing output data which can reduce a test time and a packet command driving type memory device with a pre-fetched data output structure.

It is another object of the present invention to provide a method for compressing output data which can grasp an address which a fail was produced when a fail is produced in a memory device and a packet command driving type memory device with a pre-fetched data output structure.

It is another object of the present invention to provide a packet command driving type memory device which can output data selectively in the time of a normal operation and a DA mode test by adding a circuit that can discriminate a kind of data to a front stage of a shift register of a data input, output part.

To achieve the object of the present invention, a method for compressing output data of this invention is characterized to write first data of a certain bit in a corresponding address of core cell regions, read the first data of a certain bit written in the address, compare the written data and the read data by dividing it to an upper certain bit and a lower certain bit, generate compressed data of 1 bit with an information about whether a fail is.

Also, a method for compressing output data of this invention comprises a step for reading data from a core cell region and prefetching it to a first certain bit in a normal mode; a step for writing first data of certain bit in a corresponding address of the core cell region in a test mode; a step for reading the first data of certain bit written in the address of the core

cell region and prefetching it; a step for comparing the written data of certain bit and the read data of certain bit by dividing them to data of an upper certain bit and data of a lower certain bit; a step for compressing a first error signal of certain bit to 1 bit data with an information about whether a fail is according to a comparing result and generating it; a step for selecting first data of certain bit prefetched in a normal mode or the first error signal of certain bit in a test mode according to a control signal; a step for shifting selected data of certain bit in an ascending edge and a descending edge of a clock signal and outputting them serially via a number of output pads in a normal mode; a step for shifting selected data of certain bit in an ascending edge and a descending edge of a clock signal and outputting them serially via corresponding one of a number of output pads in a test mode.

The first prefetched data of certain bit or the written and read data are 8 bits data, the 8 bits data are divided to upper 4 bits data or lower 4 bits data and compressed to 1 bit data with a fail information when it is a test mode.

Also, a packet command driving type memory device of this invention comprises a read data comparing part for receiving and comparing first data of certain bit read from a core cell region and generating compressed 2 bits data; a data input, output part for shifting the data compressed via the read data comparing part or the data read from the core cell region and transforming it to series data according to a clock signal; an interface part for outputting the data read from the data input, output part according to the clock signal serially in a packet form via an output pad.

The read data comparing part comprises a number of comparators for receiving and comparing upper or lower 4 bits data of prefetched 8 bits data according to a control signal and generating 1 bit compressed data with a fail information respectively; a selecting means for selecting the prefetched 8 bits data in a normal mode, and the compressed 8 bits data

from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal. The respective comparator comprises a first to a fourth comparing means for receiving the written 4 bits data and the read 4 bits data and comparing them by 1 bit and generating a first to a fourth comparing signal according to the control signal; a generating means for receiving the first to the fourth comparing signal generated from the first to the fourth comparing means and generating 1 bit compressed data with an information about whether a fail is.

The first to the fourth comparing means comprises a first NAND GATE for receiving corresponding 1 bit signal of the written 4 bits data and the control signal respectively; a second NAND GATE for receiving corresponding 1 bit signal of the read 4 bits data and the control signal; a third NAND GATE for receiving outputs of the first and the second NAND GATE; a first and a second NMOS Transistor having gates and drains receiving the outputs of the first and the second NAND GATE; a first and a second PMOS Transistor connected in series between a power voltage and a source of the first and the second NMOS Transistor, having gates receiving the outputs of the first and the second NAND GATE; a third PMOS Transistor having a gate receiving an output of the third NAND GATE and a source receiving a power voltage and drains connected between sources of the first and the second NMOS Transistor and drains of the first and the second PMOS Transistor; generates the first to the fourth comparing signal respectively via sources of the first and the second NMOS Transistor connected commonly and drains of the first to the third PMOS Transistor.

The generating means comprises a fourth NAND GATE for receiving the first to the fourth comparing signal generated from the first to the fourth comparing means and generating 1 bit compressed data with a fail information.

Also, The present invention comprises a number of comparators for receiving and comparing 8 bits data read from the core cell

region and generating 4 bits compressed data, receiving and comparing upper or lower 4 bits data of 8 bits prefetched data according to the control signal and generating 1 bit compressed data with a fail information respectively; a selecting means for selecting the 8 bits prefetched data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal.

A packet command driving type memory device of this invention comprises a read data comparing part having a number of comparators for receiving and comparing upper or lower 4 bits data of 8 bits prefetched data according to the control signal and generating 2 bits comparing signal, a selecting means for selecting the 8 bits prefetched data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal; a data input, output part for shifting the data compressed via the read data comparing part or the data read from the core cell region and transforming it to series data according to a clock signal; an interface part for outputting the data read from the data input, output part according to the clock signal serially via an output pad.

BRIEF DESCRIPTION OF THE INVENTION

Fig 1 shows a data pass structure in a packet command driving type memory device of the prior art.

Fig 2 shows a data pass between an interface part and a data input, output part in a packet command driving type memory device of Fig 1 in detail.

Fig 3 shows a data pass structure between a read data comparing part and an interface part and a data input, output part in a packet command driving type memory device having a read data comparing part according to an embodiment of the present

invention.

Fig 4 shows a data pass between a read data comparing part and an interface part and a data input, output part in a packet command driving type memory device of Fig 3 in detail.

Fig 5 shows each data output shift part in a data input, output part of Fig 4 in detail.

Fig 6 shows each comparator in a read data comparing part of Fig 4 in detail.

Fig 7A to Fig 7H show operation waveforms in a case that a packet command driving type memory device of this invention performs DA mode.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, a preferred embodiment of the present invention will be explained in more detail with reference to the accompanying drawings.

Fig 3 shows a data pass structure between a read data comparing part and an interface part and a data input, output part in a packet command driving type memory device having a read data comparing part according to an embodiment of the present invention. A data pass of a packet command driving type memory device according to an embodiment of the present invention has a structure that a core cell region 100, a column control part 200, a data input, output part 300, an interface part 400, a data pad(DQA or DQB) and a read data comparing part 500 for outputting data read in a normal mode or compressed data having a fail information when it is a DA mode test are arranged between the column control part 200 and the data input, output part 300.

Fig 4 shows B part(a dot line part) in a data pass structure of Fig 3 in detail, is a drawing that shows a pass that data from the core cell region 100 to an output pad(DQ) are outputted selectively via the read data comparing part 500 when it is a

normal operation or a DA mode test.

Referring to Fig 4, in a memory device according to an embodiment of the present invention, the read data comparing part 500 comprises a number of comparators 501-508 for receiving 8 bits data RD<0:7> read from the core cell region 100 according to a control signal(S_DATEST) when it is a DA mode test, compressing upper 4 bits data RD<0:3> and lower 4 bits data RD<4:7> and generating 1 bit data error<0> - error<7> having an information about whether a fail is, multiplexers 509-512 for selecting the 8 bits data RD<0:7> read from the core cell region 100 when it is a normal mode or data error<0:7> compressed from the comparators 501-508 when it is a DA mode test according to the control signal(S_DATEST).

Hereinafter, a data pass operation of a memory device of this invention having the above-mentioned structure will be explained in more detail.

First of all, a control signal(S_DATEST) in a low state is inputted from the outside when it is a normal mode and thereby the comparators 501-508 are disabled, the multiplexers 509-512 select the 8 bits data RD<0:7> read from the core cell region 100 being inputted to a first input terminal IO according to the control signal(S_DATEST), data New RD<0:7> being outputted from the multiplexers 509-512 are transformed to series data via shift registers 301-304 of the data input, output part 300. At this time, Referring to Fig 5 that shows respective shift registers 301-304 in detail, even data New RD<0, 2, 4, 6> of the data New RD<0:7> being transferred via the multiplexers 509-512 are shifted via shift registers 301-1, 302-1, 303-1, 304-1 for even data according to a clock signal, odd data New RD<1, 3, 5, 7> are shifted via shift registers 301-2, 302-2, 303-2, 304-2 for odd data.

Data transformed in series via shift registers 301-304 of the data input, output part 300 are synchronized to a clock signal TestClkR via a multiplexer and drivers 401-404 of the interface part 400 and outputted serially via respective output

pads (DQA0-DQA7 or DQB0-DQB7).

That is, by that even data being transferred via each shift register for even number of the shift registers 301-304 are transferred to a corresponding data pad via the interface part 400 in an ascending edge of the clock signal TestClkR, that odd data being transferred via a shift register for odd are transferred to a corresponding data pad via the interface part 400 in a descending edge of the clock signal TestClkR, 8 bits series data are transferred serially in a packet form via respective output pads (DQA0-DQA7 or DQB0-DQB7) during 4 clocks.

On one hand, as the control signal(S_DATEST) is transited to a high state when it is a DA mode test and inputted to an enable terminal(EN) of data comparators 501-508, the data comparators 501-508 are enabled. The data comparators 501-508 receive 8 bits data read and prefetched from the core cell region 100 by 4 bits and compress them via the respective data comparators 501-508 and generate compressed 1 bit data error<0> - error<7> having an information about whether a fail is.

That is, the comparators 501, 503, 505, 507 receive upper 4 bits data RD<0:3> of 8 bits data read from the core cell region 100 respectively and generate 1 bit compressed data error<0>, error<2>, error<4>, error<6>, the comparators 502, 504, 506, 508 receive lower 4 bits data RD<4:7> respectively and generate 1 bit compressed data error<1>, error<3>, error<5>, error<7>. As each comparing block of the read data comparing part 500 is arranged in response to the respective shift registers 301-304 of the data input, output part 300, 4 packet data read respectively by 8 bits in response to adjacent 4 data pads are compared via adjacent 4 comparing blocks of the read data comparing part 500 as drawn Fig 4, thereby data which are compressed by 1 bit are generated. Accordingly, 8 bits data are transformed to series data via one corresponding shift register 301 of 4 adjacent shift registers 301-304 of the data input, output part 300.

Therefore, as 2 comparators of each comparing block of each read data comparing part 500 receive 8 bits data and generate 2 bits compressed data, respective 8 bits data corresponding to the adjacent 4 data pads are divided to upper 4 bits or lower 4 bits respectively and compressed to 1 bit data error<0> - error<7> via comparators 501, 502, 503, 504, 505, 506, 507, 508 of each comparing block and thereby 8 bits compressed data error<0:7> are generated. Accordingly, 32 bits data being read respectively by 8 bits in response to the adjacent 4 data pads and compressed to 8 bits compressed data error<0:7> and outputted only to a second input terminal I1 of a multiplexer 509 arranged in a corresponding comparing block of respective comparing blocks of the read data comparing part 500.

The multiplexer 509 selects the data error<0:7> compressed via the comparators 501-508 according to the control signal(S_DATEST), the data New RD<0:7> selected via the multiplexer 509 are shifted to parallel data via the shift register 301, transformed to series data via a multiplexer and a driver of the interface part 400 and outputted via one corresponding output pad DQB0 of adjacent 4 pads DQB0-DQB3. At this time, as a second input terminal I2 of multiplexers 510-512 is grounded and transfers data New RD<0:7> in a low state to shift registers 302-304 according to the control signal(S_DATEST), it doesn't affect to redundant 3 data pads DQ1-DQ3 of adjacent 4 data pads.

Accordingly, whether a fail is is decided by using 8 bits data being outputted serially via an output pad DQB0 when it is a DA mode test.

Fig 5 shows one example of shift registers 301-304 of a data input, output part in a memory device having a prefetched data output structure according to the present invention in detail. Shift registers 301-304 according to the present invention comprise a first shift register (301-1 - 304-1) for even number data for shifting even data of 8 bits data New RD<0:7> being inputted via multiplexers 509-512 in an ascending edge of a

clock signal TestClkR, a second shift register (301-2 - 304-2) for even number data for shifting odd data of 8 bits data New RD<0:7> being inputted via the multiplexers 509-512 in a descending edge of a clock signal TestClkR.

Fig 6 shows an example of respective comparators 301-304 in a memory device according to the present invention, is explained with reference to a comparator 301.

Referring to Fig 6, the read data comparing part 500 of the present invention comprises a number of comparators 501-508 for storing 8 bits data WD<0:7> in the core cell region 100, and then reading 8 bits data RD<0:7> immediately and comparing them by 4 bits, respective comparators 501-508 compare upper 4 bits data WD<0:3> of written 8 bits data WD<0:7> with upper 4 bits data RD<0:3> of read 8 bits data RD<0:7> or lower 4 bits data WD<4:7> of written 8 bits data WD<0:7> with lower 4 bits data RD<4:7> of read 8 bits data RD<0:7>.

This comparator 301 comprises a number of comparing means 521-524 for comparing 4 bits data WD<0:3> written or WD<4:7> with 4 bits data RD<0:3> read or RD<4:7> by 1 bit respectively, a generating means 525 for receiving an output signal of the numbers of comparing means 521-524 and generating 1 bit compressed data with an information about whether a fail is. The comparing means 521-524 comprise a first NAND GATE 526 for receiving a corresponding 1 bit signal of the 4 bits data WD<0:3> written and a control signal(S_DATEST) being inputted as an enable signal EN, a second NAND GATE 527 for receiving a corresponding 1 bit signal of the 4 bits data RD<0:3> read and a control signal(S_DATEST) being inputted as an enable signal EN, a first NMOS Transistor 528 having a gate receiving an output of the second NAND GATE 527 and a drain receiving an output of the first NAND GATE 526, a second NMOS Transistor 529 having a gate receiving an output of the first NAND GATE 526 and a drain receiving an output of the second NAND GATE 527, a first and a second PMOS Transistor 530, 531 having gates receiving output signals of the first and the second NAND GATE 526, 527, being

connected between a power voltage Vcc and sources of the first and the second NMOS Transistor 528, 529 in series, a third NAND GATE 532 for receiving the output signals of the first and the second NAND GATE 526, 527, a third PMOS Transistor 533 having a gate receiving an output of the third NAND GATE and a source receiving a power voltage, a drain connected between sources of the first and the second NMOS Transistor 528, 529 and drains of the first and the second PMOS Transistor 530, 531.

The comparing means 521-524 generate a first comparing signal OUT1 to a fourth comparing signal OUT4 via the sources of the first and the second NMOS Transistor 528, 529 and the drains of the first to the third PMOS Transistor 530, 531, 533.

The generating means 525 receives the first to the fourth comparing signal OUT1-OUT4 and generates 1 bit compressed data ERROR<0:7> having an information about whether a fail is.

Hereinafter, an operation of each comparator of the present invention having a composition as described above will be explained.

In a case that 1 bit read data and 1 bit written data inputted to each comparator are same, for example, In a case that they are same as '0', all the outputs of the first and the second NAND GATE 526, 527 become a high state, the first and the second NMOS Transistor 528, 529 are turned on, an output of a NAND GATE 532 receiving the outputs of the first and the second NMOS Transistor 528, 529 becomes a low state and a PMOS Transistor 533 is turned on. Therefore, all the comparing means 521-524 output comparing signals OUT1-OUT4 in a high state, compressed data error<0:7> in a low state via a NAND GATE 525 of the generating means respectively.

On one hand, in the case that 1 bit read data and 1 bit written data inputted to each comparator are same as '1', as a control signal(S_DATEST) which is an enable signal EN is in a high state when it is a DA mode test, all the outputs of the first and the second NAND GATE 526, 527 become a high state, the first and the second NMOS Transistor 528, 529 are turned off according

to this, PMOS Transistors 530, 531 are turned on. Accordingly, the first to the fourth comparing signal OUT1-OUT4 being outputted from the comparing means 521-524 of each comparator become a high state and output compressed data error<0:7> in a low state via a NAND GATE of the generating means 525.

Next, in the case that 1 bit read data and 1 bit written data are different each other, for example, in the case that the written data WD are in a high state and the read data RD are in a low state, the first NMOS Transistor 528 is turned off and the second NMOS Transistor 529 is turned on, on the contrary, in the case that the written data WD are in a low state and the read data RD are in a high state, the first NMOS Transistor 528 is turned on and the second NMOS Transistor 529 is turned off, thereby the third PMOS Transistor 533 is turned off, the first PMOS Transistor 530 and the second PMOS Transistor 531 being not turned on.

Accordingly, the comparing means 521-524 of each comparator generate comparing signals OUT1-OUT4 in a low state respectively, output 1 bit compressed data error<0:7> by that an output of a NAND GATE of the generating means 525 receiving these becomes a high state.

As described above, the comparing means 521-524 of each comparator compare the written 1 bit data with the read 1 bit data, perform a logic operation such as an Exclusive NOR GATE that generates a high state signal in the case that two inputs are same, a low state signal in the case that two inputs are different each other.

The present invention compares upper or lower 4 bits data of 8 bits data written in the core cell region 100 with upper or lower 4 bits data of 8 bits data read from the core cell region 100 via the read data comparing part 500 and generates 1 bit compressed data error<0> - error<7> having an information about whether a fail is respectively. The 8 bits error data error<0:7> that the 4 bits data having an information about whether a fail is compressed by 1 bit are outputted via a DQB0 pad.

At this time, in the case that 1 bit compressed data error<0> - error<7> are in a low state, it is decided that a fail isn't generated in a core cell region of 4 bits corresponding to respective 1 bit compressed data, if 1 bit compressed data error<0> - error<7> are in a high state, it is decided that a fail is generated in a core cell region of 4 bits corresponding to respective 1 bit compressed data.

For example, in the case that error<0> is in a high state, it is decided that a fail is generated in a core cell region 100 corresponding to an address that 4 bits data corresponding to error<0> of the core cell region 100 are read, in the case that error<7> is in a high state, it is decided that a fail is generated in the core cell region 100 corresponding to an address that 4 bits data corresponding to error<7> of the core cell region 100 are read. Therefore, as this invention writes 8 bits data in a core cell region 100 corresponding to a predetermined address, and then reads 8 bits data from the region corresponding to the address of the core cell region 100 and compares them respectively by a unit of 4 bits and generates 1 bit compressed data with a fail information, one can know exactly where of a memory cell region a fail is generated.

Although the read data comparing part according to an embodiment of this invention isn't drawn, as it stores 8 bits data WD<0:7> written in a core cell region 100, compares them with 8 bits data RD<0:7> read from the core cell region 100 later.

As explained in detail above, as a method for compressing data of this invention compares whether 8 bits written data and 8 bits read data are same in a unit of upper 4 bits or lower 4 bits and compresses and generates them as 1 bit data with a fail information, it is possible to test a large amount of devices, there is an advantage that a test time can be reduced as well as a unit cost of test can be saved. Also, there is an advantage that a repair is easy by judging exactly where of a core cell region a fail is generated by using compressed data.

And, the present invention can be realized variously in a

changed form within the scope that doesn't depart from the point of this invention.

WHAT IS CLAIMED IS

1. A method for compressing output data is characterized to write first data of a certain bit in a corresponding address of core cell regions, read the first data of a certain bit written in the address, compare the written data and the read data by dividing it to an upper certain bit and a lower certain bit, generate compressed data of 1 bit with an information about whether a fail is.

2. A method for compressing output data comprising :
a step for reading data from a core cell region and prefetching it to a first certain bit in a normal mode;
a step for writing first data of certain bit in a corresponding address of the core cell region in a test mode;
a step for reading the first data of certain bit written in the address of the core cell region and prefetching it;
a step for comparing the written data of certain bit and the read data of certain bit by dividing them to data of an upper certain bit and data of a lower certain bit;
a step for compressing a first error signal of certain bit to 1 bit data with an information about whether a fail is according to a comparing result and generating it;
a step for selecting first data of certain bit prefetched in a normal mode or the first error signal of certain bit in a test mode according to a control signal;
a step for shifting selected data of certain bit in an ascending edge and a descending edge of a clock signal and outputting them serially via a number of output pads in a normal mode;
a step for shifting selected data of certain bit in an ascending edge and a descending edge of the clock signal and outputting them serially via corresponding one of a number of output pads in a test mode.

3. The method for compressing output data as clamed in clame 2, wherein the first prefetched data of certain bit or the written and read data are 8 bits data, the 8 bits data are divided to upper 4 bits data or lower 4 bits data and compressed to 1 bit data with a fail information when it is a test mode.

4. A packet command driving type memory device comprising :
a read data comparing part for receiving and comparing first data of certain bit read from a core cell region and generating compressed 2 bits data;
a data input, output part for shifting the data compressed via the read data comparing part or the data read from the core cell region and transforming it to series data according to a clock signal;
an interface part for outputting the data read from the data input, output part according to the clock signal serially in a packet form via an output pad.

5. The packet command driving type memory device as claimed in claim 4, wherein the first prefetched data of certain bit are 8 bits prefetched data, the 8 bits data are divided into upper 4 bits data or lower 4 bits data, the upper or the lower 4 bits data are compressed to 1 bit signal.

6. The packet command driving type memory device as claimed in claim 4, wherein the read data comparing part comprises :
a number of comparators for receiving and comparing upper or lower 4 bits data of prefetched 8 bits data according to a control signal and generating 1 bit compressed data with a fail information respectively;
a selecting means for selecting the prefetched 8 bits data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators

in a test mode according to the control signal.

7. The packet command driving type memory device as claimed in claim 6, wherein the respective comparator comprises :
a first to a fourth comparing means for receiving the written 4 bits data and the read 4 bits data and comparing them by 1 bit and generating a first to a fourth comparing signal according to the control signal;
a generating means for receiving the first to a fourth comparing signal generated from the first to a fourth comparing means and generating 1 bit compressed data with an information about whether a fail is.

8. The packet command driving type memory device as claimed in claim 7, wherein the first to the fourth comparing means comprises :
a first NAND GATE for receiving corresponding 1 bit signal of the written 4 bits data and the control signal respectively;
a second NAND GATE for receiving corresponding 1 bit signal of the read 4 bits data and the control signal;
a third NAND GATE for receiving outputs of the first and the second NAND GATE;
a first and a second NMOS Transistor having gates and drains receiving the outputs of the first and the second NAND GATE;
a first and a second PMOS Transistor connected in series between a power voltage and a source of the first and the second NMOS Transistor, having gates receiving the outputs of the first and the second NAND GATE;
a third PMOS Transistor having a gate receiving an output of the third NAND GATE and a source receiving a power voltage and drains connected between sources of the first and the second NMOS Transistor and drains of the first and the second PMOS Transistor;

generates the first to the fourth comparing signal respectively via sources of the first and the second NMOS Transistor connected commonly and drains of the first to the third PMOS Transistor.

9. The packet command driving type memory device as claimed in claim 7, wherein the generating means comprises a fourth NAND GATE for receiving the first to the fourth comparing signal generated from the first to the fourth comparing means and generating 1 bit compressed data with a fail information.

10. A packet command driving type memory device comprising :
a number of comparators for receiving and comparing 8 bits data read from the core cell region and generating 4 bits compressed data, receiving and comparing upper or lower 4 bits data of 8 bits prefetched data according to the control signal and generating 1 bit compressed data with a fail information respectively;
a selecting means for selecting the 8 bits prefetched data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal.

11. A packet command driving type memory device comprising :
a read data comparing part having a number of comparators for receiving and comparing upper or lower 4 bits data of 8 bits prefetched data according to the control signal and generating 2 bits comparing signal, a selecting means for selecting the 8 bits prefetched data in a normal mode, and the compressed 8 bits data from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal;
a data input, output part for shifting the data compressed via

the read data comparing part or the data read from the core cell region and transforming it to series data according to a clock signal;

an interface part for outputting the data read from the data input, output part according to the clock signal serially via an output pad.

ABSTRACT

The present invention relates to a packet command driving type memory device, a method for compressing output data according to the present invention is characterized to write first data of a certain bit in a corresponding address of core cell regions, read the first data of a certain bit written in the address, compare the written data and the read data by dividing it to an upper certain bit and a lower certain bit, generate compressed data of 1 bit with an information about whether a fail is.

FIG.1

(PRIOR ART)

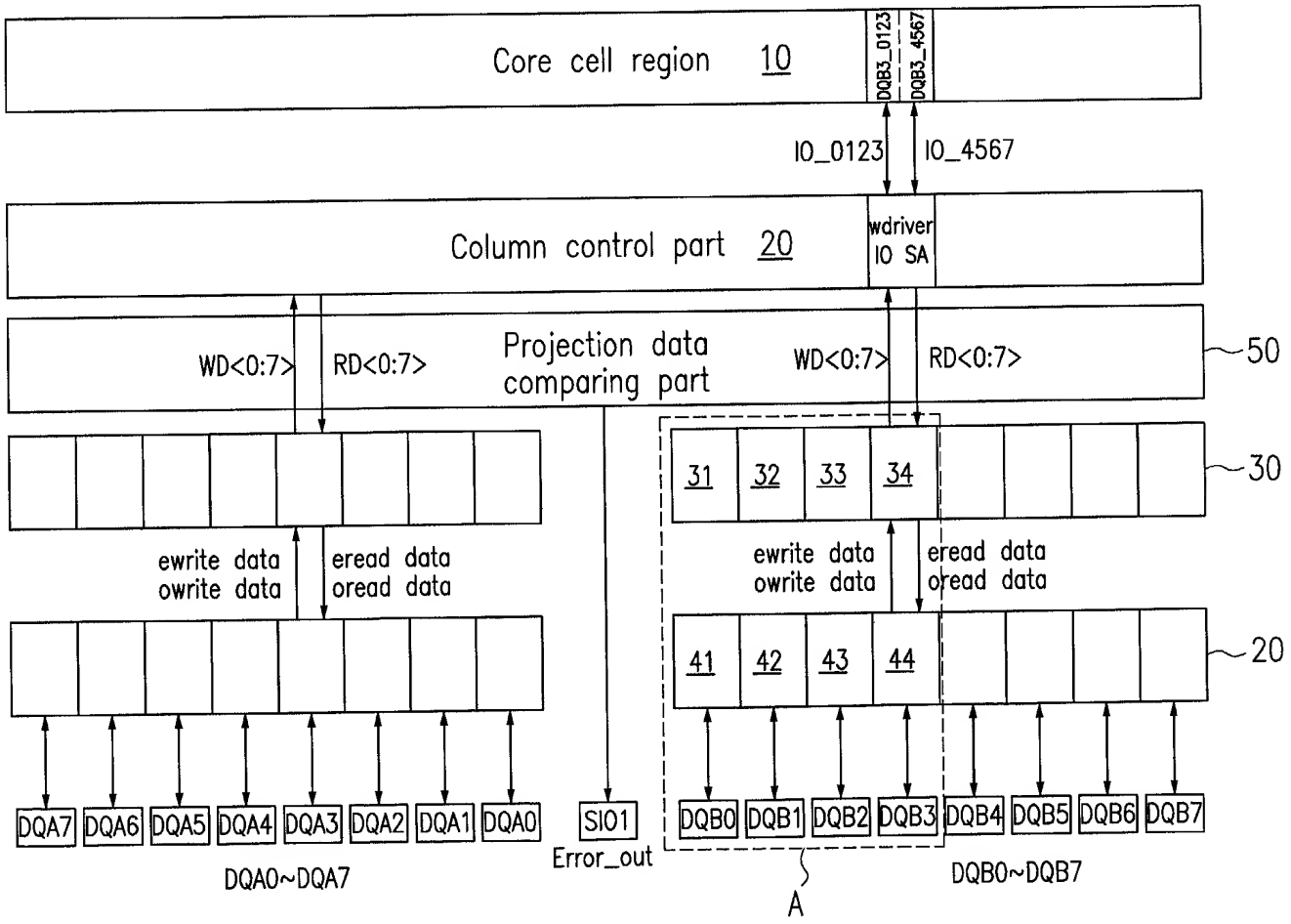

FIG.2
(PRIOR ART)

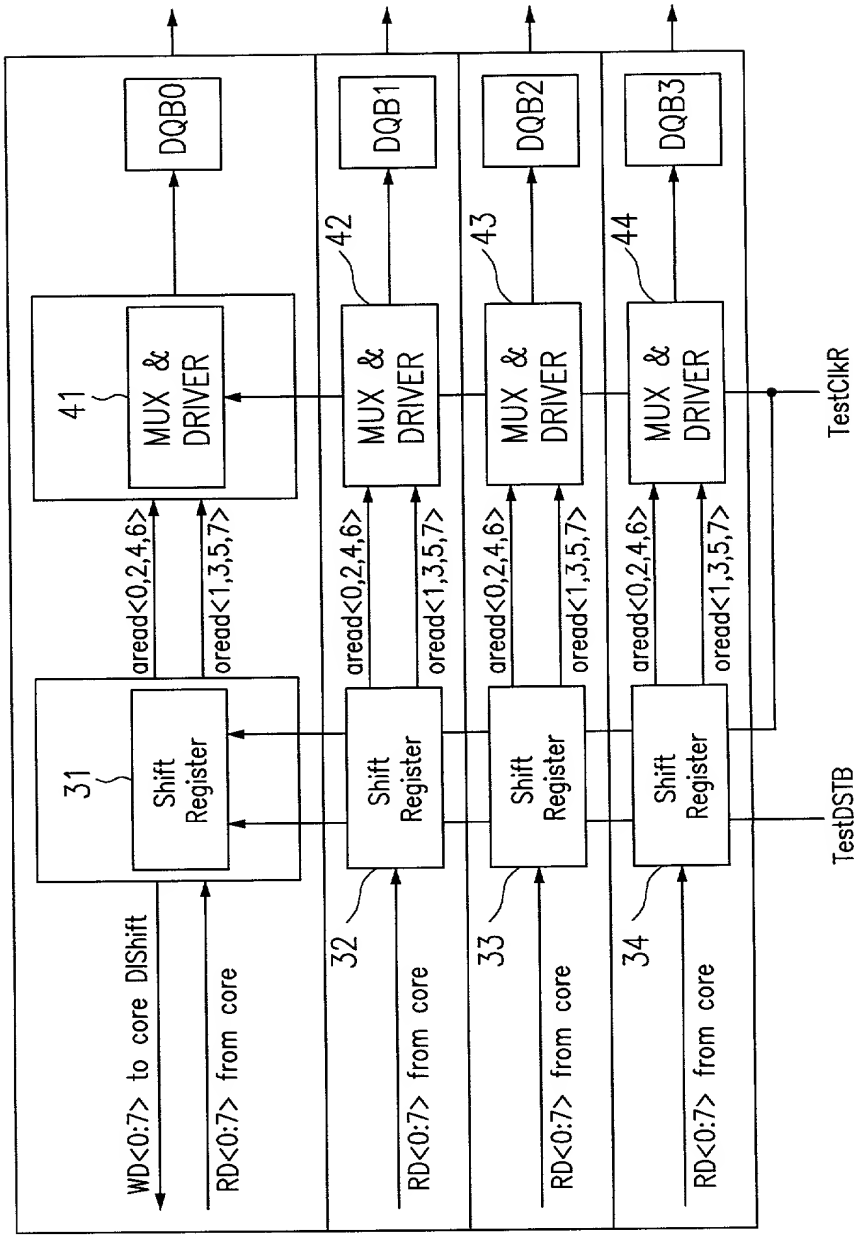

FIG.3

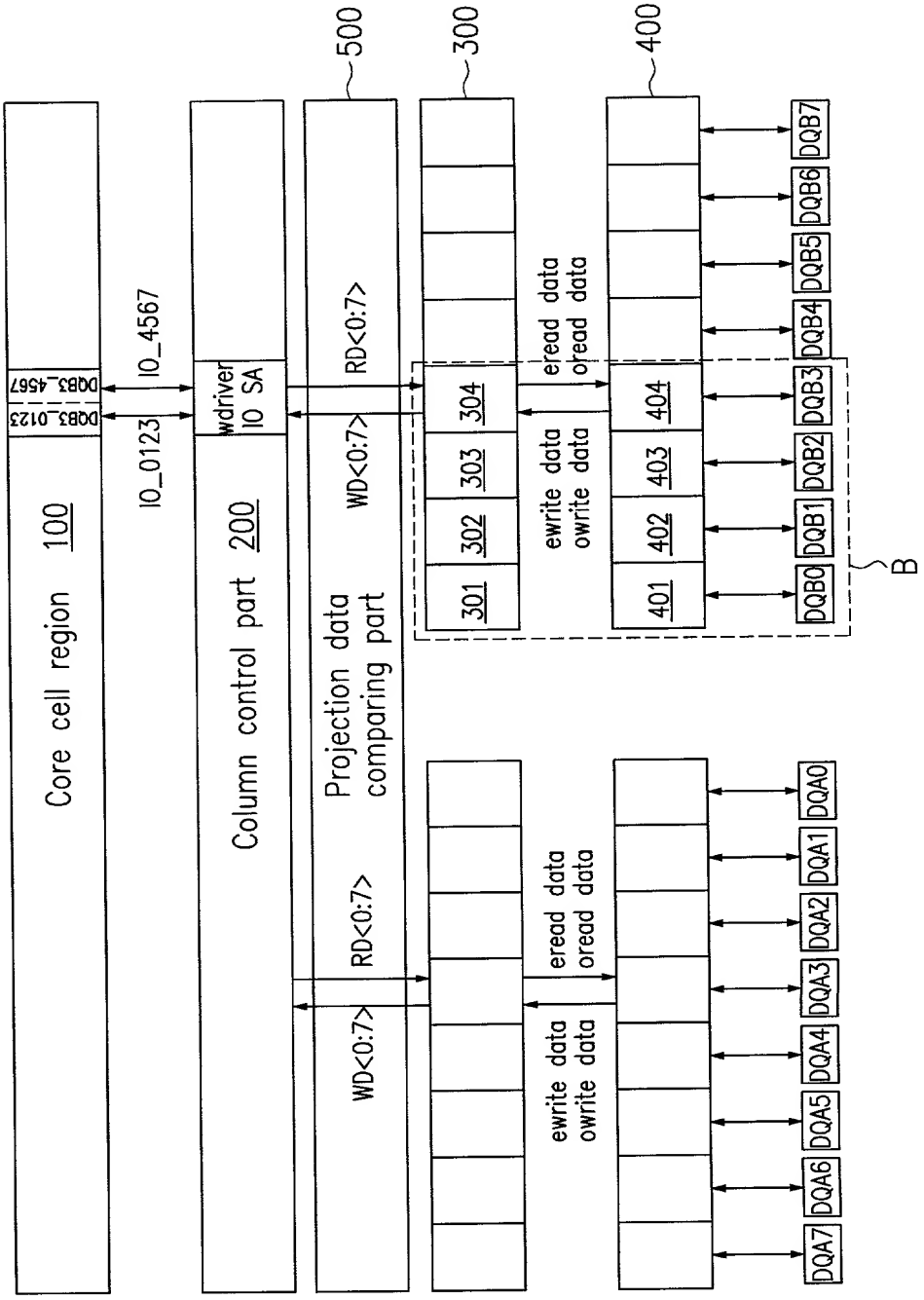
Core cell region 100
DQB3_4567
DQB3_0123
IO_4567
IO_0123
Column control part 200
wdriver
IO SA
Projection data comparing part
RD<0:7>
WD<0:7>
500
300
400
301
302
303
304
401
402
403
404
ewrite data
owrite data
eread data
oread data
DQB0
DQB1
DQB2
DQB3
DQB4
DQB5
DQB6
DQB7
DQA0
DQA1
DQA2
DQA3
DQA4
DQA5
DQA6
DQA7
B

FIG.4

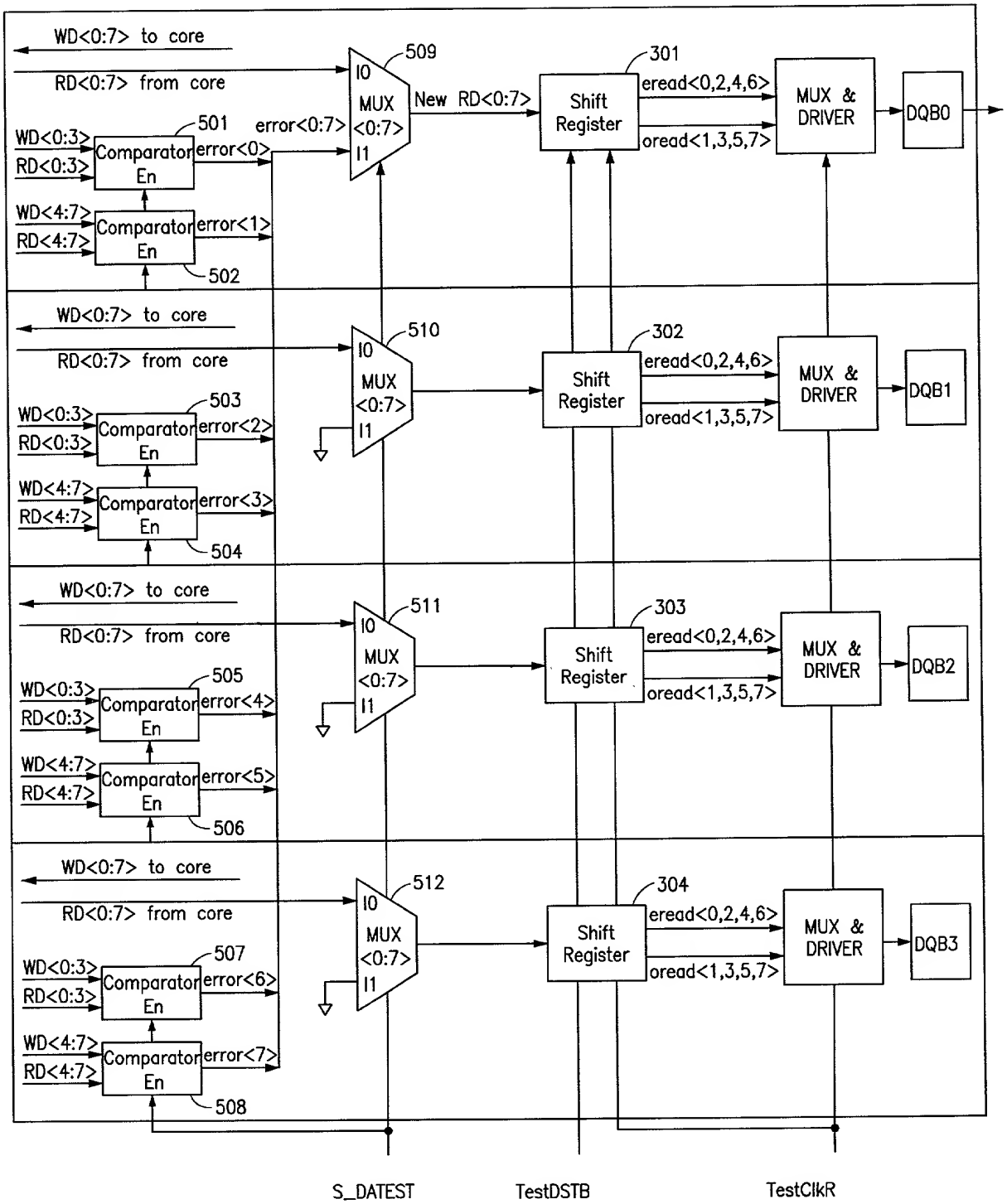
WD<0:7> to core
RD<0:7> from core
509
I0
MUX
<0:7>
I1
New RD<0:7>
301
Shift Register
eread<0,2,4,6>
oread<1,3,5,7>
MUX & DRIVER
DQB0
WD<0:3>
RD<0:3>
501
Comparator En
error<0:7>
error<0>
WD<4:7>
RD<4:7>
Comparator En
error<1>
502
WD<0:7> to core
RD<0:7> from core
510
I0
MUX
<0:7>
I1
302
Shift Register
eread<0,2,4,6>
oread<1,3,5,7>
MUX & DRIVER
DQB1
WD<0:3>
RD<0:3>
503
Comparator En
error<2>
WD<4:7>
RD<4:7>
Comparator En
error<3>
504
WD<0:7> to core
RD<0:7> from core
511
I0
MUX
<0:7>
I1
303
Shift Register
eread<0,2,4,6>
oread<1,3,5,7>
MUX & DRIVER
DQB2
WD<0:3>
RD<0:3>
505
Comparator En
error<4>
WD<4:7>
RD<4:7>
Comparator En
error<5>
506
WD<0:7> to core
RD<0:7> from core
512
I0
MUX
<0:7>
I1
304
Shift Register
eread<0,2,4,6>
oread<1,3,5,7>
MUX & DRIVER
DQB3
WD<0:3>
RD<0:3>
507
Comparator En
error<6>
WD<4:7>
RD<4:7>
Comparator En
error<7>
508
S_DATEST
TestDSTB
TestClkR

FIG.5

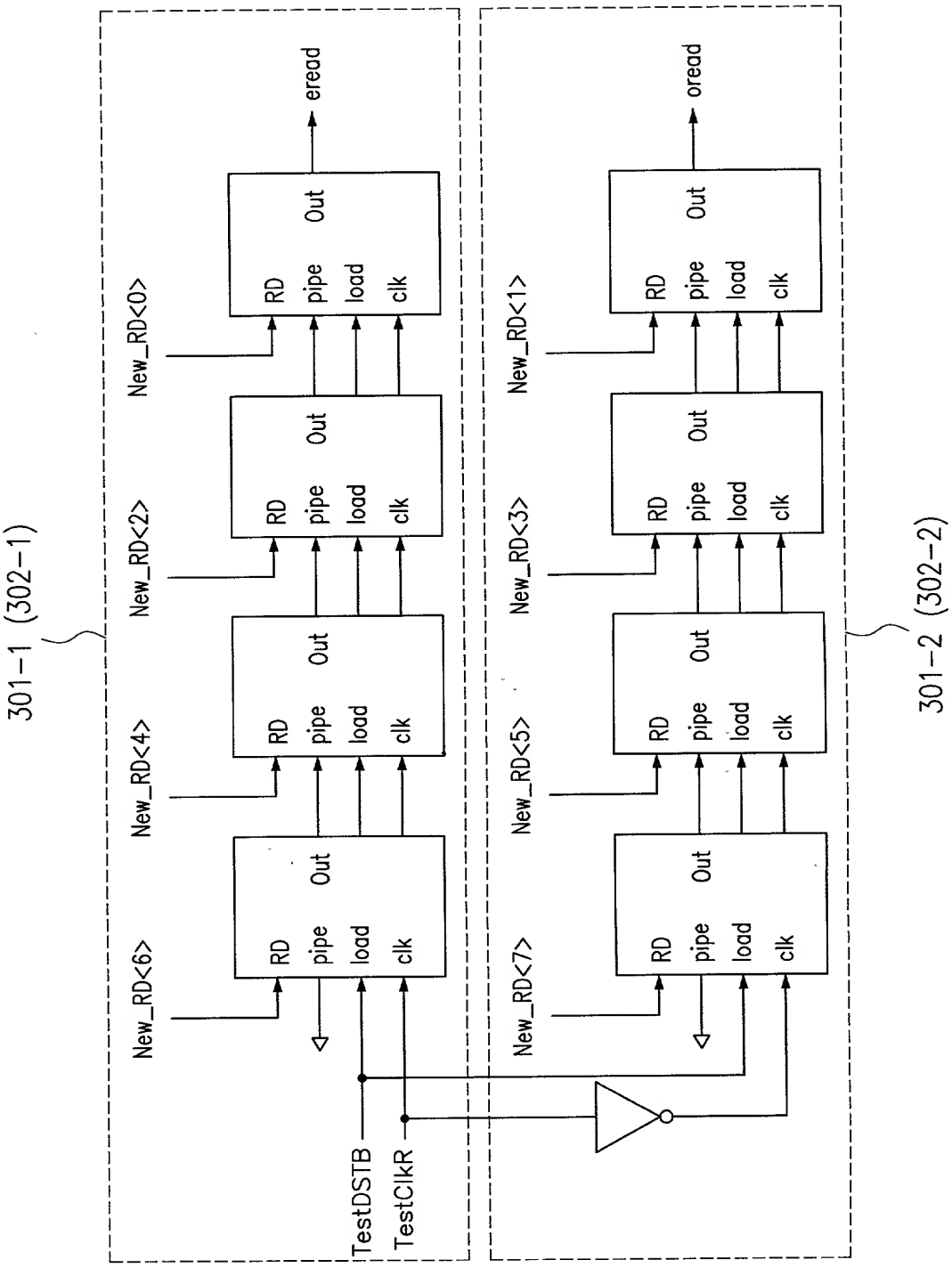
301-1 (302-1)
301-2 (302-2)
New_RD<0>
New_RD<1>
New_RD<2>
New_RD<3>
New_RD<4>
New_RD<5>
New_RD<6>
New_RD<7>
RD
pipe
load
clk
Out
eread
oread
TestDSTB
TestClkR

FIG.6

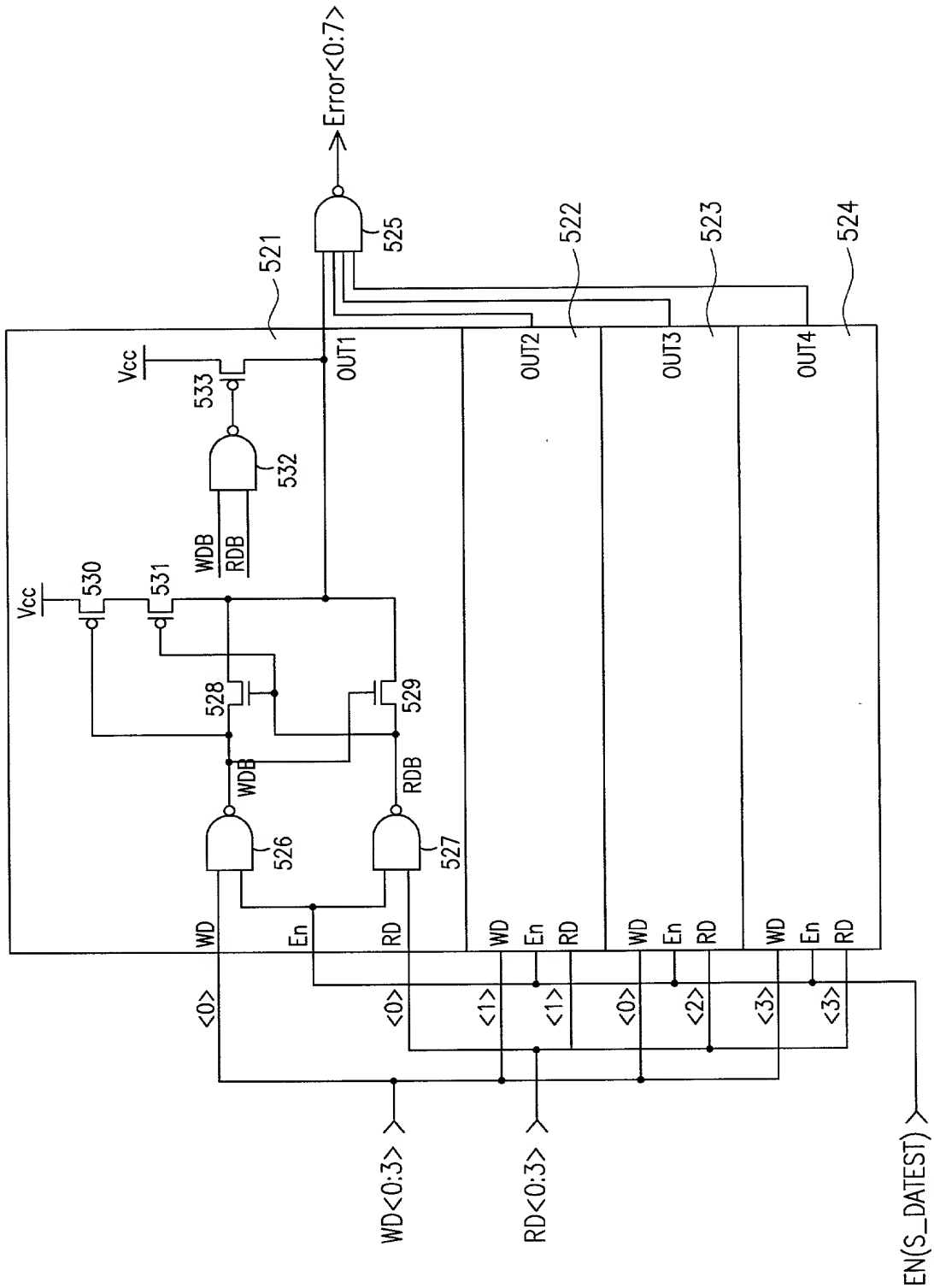
Error<0:7>
525
521
522
523
524
OUT1
OUT2
OUT3
OUT4
Vcc
533
532
WDB
RDB
530
531
528
529
526
527
WD
En
RD
<0>
<1>
<2>
<3>
WD<0:3>
RD<0:3>
EN(S_DATEST)

FIG.7A

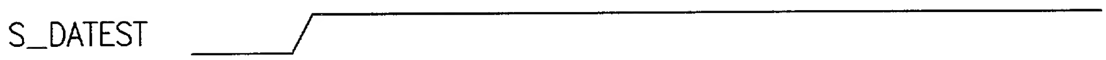

FIG.7B

FIG.7C

FIG.7D

FIG.7E

FIG.7F

FIG.7G

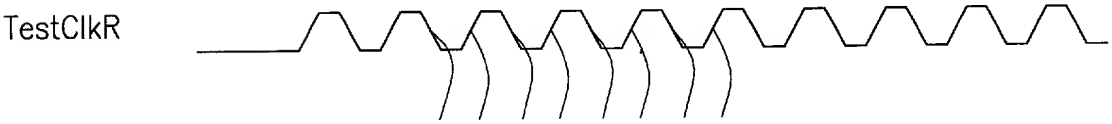

FIG.7H